

Appln No. 10/037,671  
Amdt date August 30, 2005  
Reply to Office action of March 30, 2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1.-7. (Canceled)

Claim 8. (Original) A digital clock recovery unit with harmonic lock prevention, comprising:

a phase generator receiving a clock signal and generating multiple phase-shifted versions of the clock signal;

a reference loop including a reference phase detector comparing two of the phase-shifted versions of the clock signal and driving a reference selector to cause selection of phase-shifted versions of the clock signal phase-shifted a predetermined amount, the reference loop forming a reference selection signal indicating a clock period of the clock signal;

a clock recovery loop including a phase detector comparing a phase-shifted version of the clock signal with a data signal, the phase detector driving a selector to cause selection of a phase-shifted version of the clock signal having a constant phase with respect to the data signal;

the selector of the clock recovery loop limiting the selection of the phase-shifted version of the clock signal having a constant phase with respect to the data signal based on the reference selection signal.

Appln No. 10/037,671

Amdt date August 30, 2005

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Claims 9.-10. (Canceled)

11. (Currently Amended) A method of recovering a clock signal from a data stream comprising:

providing a reference clock signal approximate an expected frequency of the clock signal to a delay line;

determining a length of the delay line corresponding to a period of the reference clock signal;

iteratively selecting a recovered clock signal from the delay line based on a comparison of the recovered clock signal with a data signal, the recovered clock signal limited to a section of the delay line corresponding to the period of the reference clock signal;

wherein determining a length of the delay line corresponding to a period of the reference clock signal comprises comparing a first clock signal from a variable position on the delay line with a second clock signal from a fixed position on the delay line and adjusting the position of the variable position until the first clock signal and the second clock signal have a constant phase relationship;

~~The method of claim 10~~ wherein the constant phase relationship is zero phase difference.

Claim 12. (Original) The method of claim 11 wherein the difference in position between the fixed position and the variable position indicates the length of the delay line corresponding to one clock period of the reference clock.

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Claim 13. (Original) The method of claim 12 wherein the recovered clock signal is limited to positions along the delay line from the fixed position to the variable position.

Claim 14. (Original) The method of claim 13 wherein the recovered clock signal is selected from positions along the delay line that vary at a substantially constant rate, whereby the recovered clock signal is offset in frequency from the reference clock signal.

Claim 15. (Original) The method of claim 13 further comprising determining a sampling clock signal using the recovered clock signal and a fraction of the difference between the fixed position and the variable position.

Claim 16. (Original) The method of claim 15 wherein the fraction is one-half.

Claim 17. (Original) The method of claim 15 wherein the sampling clock signal and the recovered clock signal have a phase difference of approximately 90 degrees.

Claims 18.-21. (Canceled)